REMARKS/ARGUMENTS

The Office Action dated September 20, 2005 has been carefully considered. Claims 1-11 are pending in the present application with claims 1 and 11 in independent form. By the present amendment claims 1, 4 and 11 have been amended to further clarify the features of the present application and claims 2 and 3 have been canceled without prejudice of disclaimer.

The Examiner objected to the specification because paragraph 0025 on page 6 recites claim element 22 as a "capacitor" and the Examiner contends that claim element 22 is clearly a comparator. Paragraph 0025 has been amended hereby to correct the error noted by the Examiner.

Accordingly, it is respectfully requested that the objection tot he specification be reconsidered and withdrawn.

Claims 1, 5, 7 and 8 have been rejected under 35 U.S.C. §102(b) as allegedly unpatentable over U.S. Patent No. 6,456,171 to Segawa.et al.

The Examiner contends that figures 11 and 22 and the relevant text related thereto of Segawa et al. disclose all of the features of claim 1 of the present application. Applicants respectfully disagree.

Claim 1, as amended herein, relates to an adjustable oscillator circuit including a timing capacitor capable of being charged or discharged at an adjustable rate, an adjustable current source coupled to the capacitor for charging or discharging the capacitor at the adjustable rate, a threshold circuit for changing a charging or discharging state of the capacitor based on a charge value of the capacitor, a threshold value in the threshold circuit for comparison with the charge value of the capacitor to determine the change of charging or discharging state, a switch in the adjustable current source operable to vary the current supplied to the capacitor and a digital to analog converter coupled to the switch and operable to receive input digital data and to provide an analog control signal to the switch to vary the current supplied to the capacitor based on the input digital data. It is noted that claim 1, as amended herein, substantially includes the subject matter of claims 2-3 which have been canceled hereby without prejudice and disclaimer.

Segawa et al. discloses a conventional voltage controlled oscillator circuit. This voltage controlled oscillator circuit includes first and second differential comparators 110 and 111, a capacitor 112 for supplying a comparison voltage Vc to the first and second comparators 110 and 111, first and second current sources 113 and 114 for charging or discharging the capacitor 112, converter circuit 115 for making each of the first and second current sources 113 and 114 generate a current proportionate to the input voltage, first and second switches 116 and 117 and inverter 118 for respectively controlling on/off of the first and second current sources 113 and 114, and latch circuit 119 for latching output signals of the first and second comparators 110 and 111 and outputting an oscillation signal of the voltage controlled oscillator circuit. See Segawa et al. Col. 3, lines 25-40 and Fig. 11.

Segawa et al., however, as understood by Applicants, does not disclose an adjustable oscillator circuit including "a switch in the adjustable current source operable to vary the current supplied to the capacitor and a digital analog converter coupled to the switch and operable to receive input digital data and to provide an analog control signal to the switch to vary the current supplied to the capacitor based on the input digital data" as recited in claim 1 of the present application.

While Segawa et al. generally discloses a voltage controlled oscillator circuit, Segawa et al. makes no mention whatsoever of a switch in the adjustable current source or a digital to analog converter at all, much less a switch in the adjustable current source operable to vary the current supplied to the capacitor and a digital to analog converter coupled to the switch that receives input digital data and provides an analog control signal to the switch to vary the current supplied to the capacitor based on the input digital data.

The Examiner, with regard to original claims 2-4, concedes that Segawa et al. is silent as to the construction of the variable current sources, but contends that Japanese Patent Publication No. 01157612 to Daisuke discloses a conventional variable current source that can be composed of a passive element coupled to a switching element and is for setting a minimum amount of current. The Examiner also notes that Daisuke also discloses a current mirror that parallels that of the present invention. The Examiner contends that it would have been obvious to replace the current sources of Segawa et al. with those disclosed in Daisuke because as the Segawa et al.

reference is silent on the exact structure of the current sources and shows current sources as conventional current sources and that one of ordinary skill in the art would have been motivated to use any art-recognized equivalent variable current source. Applicants respectfully disagree.

Daisuke is in the Japanese language and no English language translation of Daisuke or any portion thereof has been provided by the Examiner. The Examiner contends that Daisuke illustrates a conventional variable current source 1 in Figure 1 that can be composed of a passive element 15 coupled to a switching element and is for setting a minimum amount of current. Figure 1 of Daisuke, however, does not appear to include an element 15. Figure 2 does appear to illustrate an element 15, which appears to be a resistor, however, there is no variable current source 1 illustrated in Figure 2. Further, since Daisuke is in the Japanese language it is impossible to tell exactly what the relationship is between Figures 1 and 2.

In addition, it is respectfully submitted that there is no suggestion in either Segawa et al., Daisuke or the art as a whole to combine the variable current source allegedly disclosed in Daisuke with the oscillator circuit of Segawa et al. As the Examiner notes, Segawa et al. is silent as to the structure of the current sources therein. Further, Daisuke does not appear to provide any teaching or suggestion as to why one may be motivated to utilize the current source therein with the oscillator circuit of Segawa et al.

Further, the Examiner has not indicated any other motivation to combine the alleged current source of Daisuke with the oscillator circuit of Segawa et al. Indeed, the Examiner indicates that since Segawa et al. is silent as to the structure of the variable current source, any art recognized equivalent variable circuit source may be used. The Examiner, thus, apparently concedes that there is no motivation to use the specific current source allegedly disclosed in Daisuke.

In addition, the Examiner concedes that the Vin signal of Segawa et al. is an analog signal, however, the Examiner contends that digital controls are well known in the art for setting an analog value used in a VCO via a D to A converter and thus the Examiner takes official notice of this. The Examiner further contends that it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a D to A converter to come up with the analog signal Vin in Segawa to allow for the use of digital control and digital signals to control

the VCO. The Examiner also contends that one of ordinary skill in the art would have been motivated to provide a D to A converter so as to allow for the use of a microprocessor as the ultimate source of the Vin signal so as to obtain the advantage of changing or providing programming that a microprocessor offers. Applicants respectfully disagree.

The Examiner has taken the position that digital controls are well known in the art for setting an analog value used in a VCO via a D to A converter, however, the Examiner has failed to identify any reference that discloses such a feature. Applicant notes that "[A]ny rejection based on assertions that a fact is well-known or is common knowledge in the art without documentary evidence to support the examiner's conclusion should be judiciously applied." In addition, "[I]t is never appropriate to rely solely on common knowledge in the art without evidentiary support in the record as the principal evidence upon which a rejection was based." See M.P.E.P. §2144.03 E. Accordingly, it is respectfully submitted that it is improper for the Examiner to take official notice of the fact that digital controls are well known in the art for setting an analog value used in a VCO via a D to A converter without supplying any documentary support for this statement.

Further, even if the use of a D to A converter is generally known, the Examiner has cited nothing in support of a contention that it is obvious to provide "a digital to analog converter coupled to the switch and operable to receive input digital data and to provide an analog control signal to the switch to vary the current supplied to the capacitor based on the input digital data, " as recited in amended claim 1 of the present application.

Accordingly, it is respectfully submitted that claim 1, and the claims depending therefrom, are patentable over the cited art for at least the reasons discussed above.

Claim 10 has been rejected under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent No. 5,850,127 to Zhu et l. in view of Segawa et al.

Claim 10, depends indirectly from claim 1. As noted above, it is believed that claim 1 is patentable over Segawa et al. for at least the reasons discussed above. Further, it is respectfully submitted that claim 1 is patentable over Segawa et al. and Zhu et al., at least because Segawa et al. and Zhu et al., either alone or in combination, fail to show or suggest the patentable features of claim 1 as discussed above.

Accordingly, it is respectfully submitted that claim 1, and the claims depending therefrom, including claim 10, are patentable over the cited art for at least the reasons discussed above.

Claims 2-4 have been rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Segawa et al. in view of Daisuke.

As noted above, claim 2-3 have been canceled herein without prejudice or disclaimer. Thus, the rejection of claims 2-3 is considered moot.

Claim 4 depends from claim 1. As noted above, it is believed that claim 1 is patentable over Segawa et al. and Daisuke at least because Segawa et al. and Daisuke, either alone or in combination, fail to show or suggest the patentable features of claim 1 as discussed above.

Accordingly, it is respectfully submitted that claim 1, and the claims depending therefrom, including claim 4, are patentable over the cited art for at least the reasons discussed above.

Claim 6 and 9 have been rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Segawa et al. in light of U.S. Patent No. 4,692,717 to Quyang et al.

Claims 6 and 9 depend indirectly from claim 1. As noted above, it is believed that claim 1 is patentable over Segawa et al. for at least the reasons discussed above. Further, it is respectfully submitted that claim 1 is patentable over Segawa et al. and Quyang et al. at least because Segawa et al. and Quyang et al. either alone or in combination, fail to show or suggest the patentable features of claim 1 as discussed above.

Accordingly, it is respectfully submitted that claim 1, and the claims depending therefrom, including claims 6 and 9, are patentable over the cited art for at least the reasons discussed above.

Claim 11 has been rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Segawa et al.

Claim 11, as amended herein, relates to a method for providing a variable frequency signal including charging or discharging a capacitor at a selected rate to obtain a variable capacitor charge value, determining when the capacitor charge value reaches a predefined value; changing the charging or discharging state of the capacitor and controlling the selected rate with

a digital value, wherein the controlling step further includes varying a current supplied to the capacitor, receiving input digital data via a digital to analog converter and providing an analog control signal from the digital to analog converter to vary the current supplied to the capacitor based on the input digital data.

The Examiner again contends that digital controls are well known in the art for setting an analog value used in a VCO via a D to A converter and takes official notice of this fact. The Examiner again also contends that it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a D to A converter to come up with the analog signal Vin in Segawa et al. to allow for the use of digital control and digital signals to control the VCO and that one of ordinary skill in the art would have been motivated to provide a D to A converter so as to allow for the use of a microprocessor as the ultimate source of the Vin signal so as to obtain the advantage of changing or providing programming that a microprocessor offers. Applicants respectfully disagree.

First, as noted above with regard to claim 1, it is believed that it is improper for the Examiner to take official notice. In addition, even if the use of digital controllers is generally know, the Examiner has cited nothing to support his contention that it would be obvious to provide a variable frequency signal including "varying a current supplied to the capacitor, receiving input digital data via a digital to analog converter and providing an analog control signal from the digital to analog converter to vary the current supplied to the capacitor based on the input digital data," as recited in claim 11 of the present application.

Accordingly, it is respectfully submitted that claim 11 is patentable over the cited art for at least the reasons noted above.

In light of the remarks and amendments made herein, it is respectfully submitted that claims 1 and 4-11 are patentable over the cited art and are in condition for allowance.

Favorable reconsideration of the present application is respectfully requested.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 21, 2005

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Name of applicant, assignee or Registered Representative

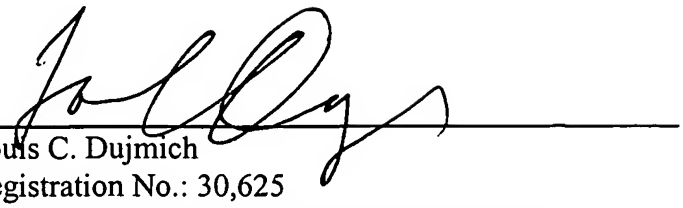
Signature

December 21, 2005

Date of Signature

LCD:KJB/jl

Respectfully submitted,



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